Fan-Out Wafer Level Packaging
Patent Landscape Analysis

November 2016
INTRODUCTION
Scope of the report

<table>
<thead>
<tr>
<th>Included in the report</th>
<th>Not included in the report</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Patents related to “Fan-Out” solutions that are embedding dies in a mold compound and are not using laminated advanced substrate for the redistribution layers (RDL).</td>
<td>• Patents related to “Fan-Out” solutions that are embedding dies in laminated materials.</td>
</tr>
<tr>
<td>Fan-Out technologies: eWLB (Infineon, Nanium, STATS ChipPAC, ASE ...), RCP (Freescale/NXP, Nepes ...), InFO (TSMC), SWIFT &amp; SLIM (Amkor), NTI/SLIT (SPIL/Xilinx), M-Series (Deca, ASE), CHIEFS &amp; CLIP (PTI), WDoD (3D PLUS), etc.</td>
<td>• Patents related to “Fan-Out” solutions where the mold compound embedding is on the top of advanced substrate (PCB type), standard or coreless.</td>
</tr>
<tr>
<td>• Patents related to other design of package.</td>
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</tbody>
</table>

**Single Chip FOWLP**

**Single chip with passives**

**Multi-Chip**

**FO WLP + Face to Face (F2F)**

**FO PoP with TMV**

**FO PoP with 2 FO Packages**

**3D PoP / Stacked dies**

**FO PoP with TMV**

**FO SiP**

**FO SiP + F2F**

**3D IC TSV interconnect**

**Interposer based**

**Embedded die**

**Coreless FC**

**Fan-In WLP**

**Leadframe (QFN,QFP )**

**WB BGA**

**FC CSP / FC BGA**
INTRODUCTION
Methodology for patent search, selection and analysis

Phase I
- Keywords and term-set definition
- Search equations / Search strategy

Phase II
- Manual screening of the results
- Patent classification
  - Relevant
  - Non relevant
- Refine search using IPC classes and citations analysis

Phase III
- Patent Segmentation
  - Patent Analysis
- Patent landscape overview
- In-depth analysis of key technology segments and key players
- Ranking of key players and key patent analysis

FamPat worldwide patent database (Questel)
Patents published up to September 2016

Manual selection
3,160+ “Fan-Out” relevant patents grouped in 1,260+ patent families
FAN-OUT PATENT LANDSCAPE OVERVIEW

Main patent applicants in FOWLP

Ranking of main patent applicants involved in fan-out wafer level packaging (according to the number of their patent families*)

• 100+ patent applicants.
• Nanium does not file any patents.
• R&D Labs have only few patents.
• Patent licensing companies (WiLAN).

* A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor. A first application is made in one country – the priority country – and is then extended to other countries.
FAN-OUT PATENT LANDSCAPE OVERVIEW

Time evolution of patent applications in FOWLP

Patent activity in the field of fan-out wafer level packaging
3,160+ patents (1,260+ patent families*), including 1,600+ granted patents and 1,200+ pending patent applications

- **First wave of patented inventions**
- **Second wave of patent filings**

The second wave of patent filings combined to an increase of patent extensions worldwide is an indication of the technology maturity and market ramping up.

<table>
<thead>
<tr>
<th>Year of application</th>
<th>Number of applications</th>
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</thead>
<tbody>
<tr>
<td>1990-2016</td>
<td>0-600</td>
</tr>
</tbody>
</table>

**Patent activity trends**
- **1990-2000**: Steady increase
- **2000-2007**: Steady decline
- **2007-2014**: Significant increase (18% CAGR)

**Innovation triggers**
- General Electric US5353498 (expired)
- MCNC / Unitive International US5892179 (expired)
- EPIC Technologies US5841193 (expired)
- Fraunhofer US6093971 (granted)

**Extension of priority patents**
- CAGR 2007-2014: 18%
- **2015-2016**: Note: The data corresponding to the year 2015 and 2016 may not be complete since most patents filed during these years are not published yet.

* A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor. A first application is made in one country – the priority country – and is then extended to other countries.

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FAN-OUT PATENT LANDSCAPE OVERVIEW

Geographic map of patenting activity of main IP players involved in FOWLP

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USA
630+ GRANTED PATENTS
360+ PENDING PATENTS

Europe
80+ GRANTED PATENTS
190+ PENDING PATENTS

Japan
35+ GRANTED PATENTS
60+ PENDING PATENTS

Taiwan
165+ GRANTED PATENTS
300+ PENDING PATENTS

China
140+ GRANTED PATENTS
70+ PENDING PATENTS

Singapore
145+ PENDING PATENTS

Europe
25+ GRANTED PATENTS
20+ PENDING PATENTS

Korea
200+ GRANTED PATENTS
145+ PENDING PATENTS

Singapore
165+ GRANTED PATENTS
300+ PENDING PATENTS
FAN-OUT IP POSITION OF MAIN PATENT ASSIGNEES

IP position vs. remaining lifetime of enforceable patents

Circle size represents the number of patent families

Polaris Innovations

Remaining lifetime of granted patents
# FAN-OUT PATENT SEGMENTATION

Patented technologies by key IP players in FOWLP

<table>
<thead>
<tr>
<th>TECHNOLOGY</th>
<th>PROCESS STEPS</th>
<th>TECHNICAL CHALLENGES</th>
<th>ARCHITECTURE</th>
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<tbody>
<tr>
<td></td>
<td>Die placement</td>
<td>Molding</td>
<td></td>
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<tr>
<td></td>
<td>Molding</td>
<td>Planarization</td>
<td></td>
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<td>RDL</td>
<td></td>
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<td>RDL</td>
<td>Foundry BEOL</td>
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<td></td>
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<td>Die shift</td>
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<td></td>
<td></td>
<td>Warpage</td>
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<td>Chip-first Face-down</td>
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<td></td>
<td>MCM (multi-chip module)</td>
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<td></td>
<td>PoP (package-on-package)</td>
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- **50+ patent families**
- **130+ patent families**


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EXCEL PATENT DATABASE
Including all Fan-Out patents analyzed in the report with technology segmentation

Multi-criteria searches and includes patent publication number, hyperlinks to the original documents, priority date, title, abstract, patent assignees, technological segments, and legal status for each member of the patent family.
MAJOR CHALLENGES FOR FAN-OUT

Technical solutions found in patent to solve warpage and die shift issues

- Hard wafer carrier (metal, glass, ceramics, silicon)
- Stress relief layer
- Pressure member (on the encapsulant)
- Better mold compound material formulation
- Better lithography equipment
- Recessed portions (in mold compound or in interconnect)
- Thermally conductive sheet
- Adaptive patterning of RDL
- Embedded units
- Fixing material
- Recessed portions in carrier substrate
- Positioning unit
- RDL before moulding the resin
- Improved alignment lithography
- Double encapsulation process

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Taiwan Semiconductor Manufacturing Company

TSMC is the main IP challenger and might change the FOWLP market landscape

- Large and young patent portfolio: 200+ granted patents, 280+ pending patents
- Strong IP leadership: Medium prior art strength index
- Limited IP blocking potential: Noticeable IP enforcement potential
- Broad technological coverage in patents
- Broad geographic coverage of patents

Patent activity in the field of fan-out wafer level packaging

- Number of patent families:
  - Earliest year of application for each patent family:
    - 1995: 0
    - 1996: 0
    - 1997: 0
    - 1998: 0
    - 1999: 1
    - 2000: 0
    - 2001: 0
    - 2002: 0
    - 2003: 0
    - 2004: 2
    - 2005: 1
    - 2006: 2
    - 2007: 3
    - 2008: 23
    - 2009: 45
    - 2010: 69
    - 2011: 8
    - 2012: 1
    - 2013: 0
    - 2014: 0
    - 2015: 0
    - 2016: 0


InFO PoP 3D-Stacking

- Copper pillars Through InFO Via (TIV)

Passive die under the AP

TSMC’s patents claim an IPD component connected under a chip into a InFO-PoP


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CONCLUSIONS

• All of major players involved in Fan-Out packaging own related patents, except Nanium.

• According to the global patenting activity, the areas of market interest for FOWLP players are mainly the USA, China, Taiwan, and Korea. Europe does not seem to be a market area of interest for Asian players (insignificant patent filings in Europe, except TSMC).

• JCET/STATS ChipPAC and TSMC are leading the FOWLP patent landscape.
  - Both companies combine a large enforceable patent portfolio with a long remaining lifetime of their patents.
  - JCET/STATS ChipPAC: strong IP position, important contribution to the prior art, formidable IP blocking potential.
  - TSMC: most prolific patent applicant, most serious IP challenger.

• Despite an unclear position in FOWLP market, Samsung has nonetheless been involved in patenting activity since 2000s and it has a noticeable IP position in the FOWLP patent landscape.

• Newcomers in FOWLP patent landscape: NCAP (National Center for Advanced Packaging), SMIC (Semiconductor Manufacturing International Corporation), HuaTian Technologies, Apple, WiLAN.

• Not yet litigation cases observed in FOWLP, but the situation could rapidly change due to the market adoption.
  - Players with strong IP position (JCET/STATS ChipPAC, TSMC, Infineon ...)
  - Apple A10 APE / TSMC InFO PoP
  - Patent licensing companies (WiLAN)