



nepes

# 2022 INTRODUCTION



Semiconductor

Artificial Intelligence

IT Materials



ABOUT  
NEPES



BUSINESS  
PORTFOLIO



CORE  
TECHNOLOGY



GLOBAL  
NEPES



CORPORATE  
CULTURE



ADVANCED  
BACK-END  
FOUNDRY

네패스의 4차원 경영은 회사명을 결정하는 그 순간부터 시작되었습니다.



어원(히브리어)

נֶפֶשׁ(nephesh)

Eternal Life / Dynamic

장수기업



## 4차원 경영이란?

젓과 꿀이 흐르는 장수 기업이 되기 위해 **창조, 혁신, 개혁** 사건과 **재미, 만족, 기쁨** 사건이 계속적으로 일어나게 하는 경영

Corporate Identity

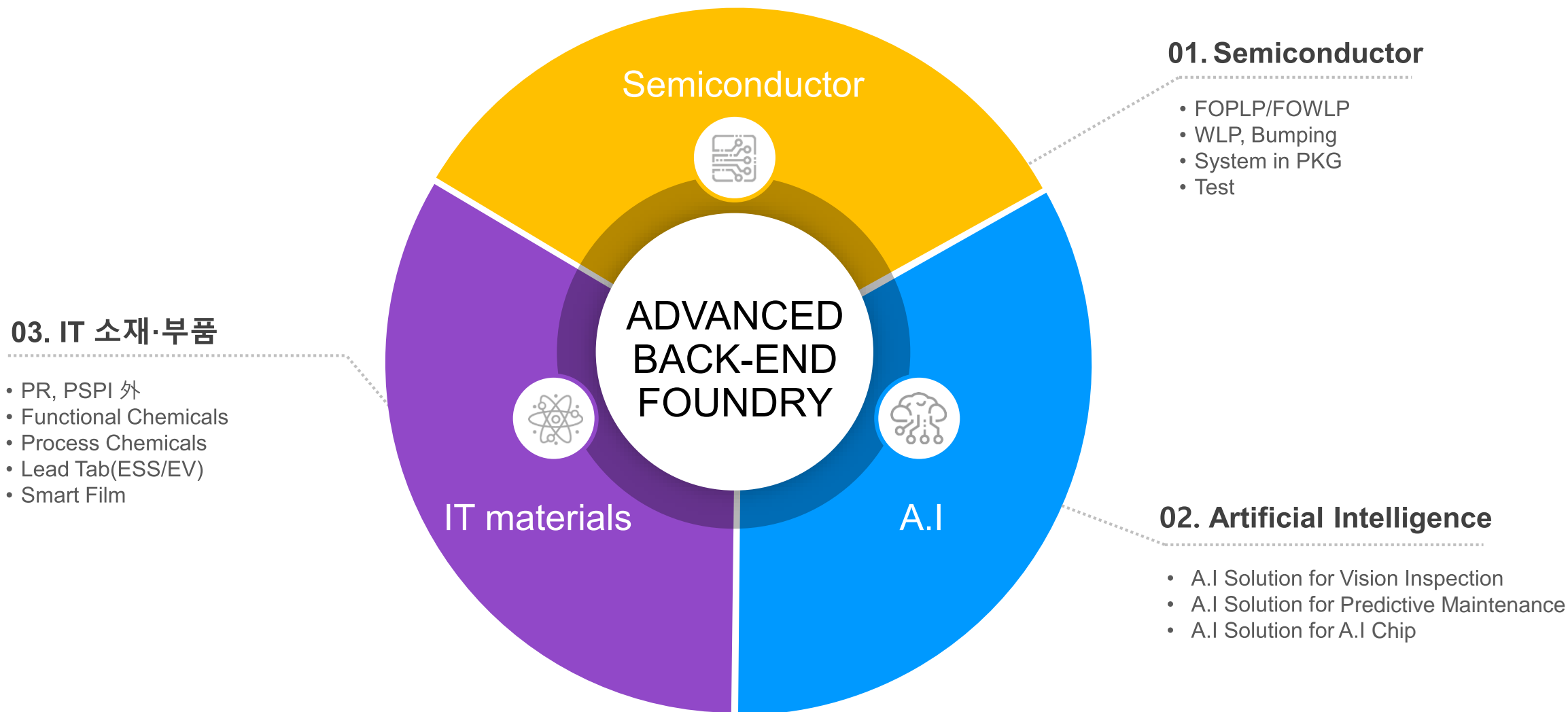


Trademark



회 사 명	주식회사 네패스
설 립 연 월	1990년 12월
상 장 연 월	1999년 12월(KOSDAQ 033640)
C E O	이병구 (Byung-Koo Lee, 李柄九)
해 외 법 인	CN, US, PHL, IDN

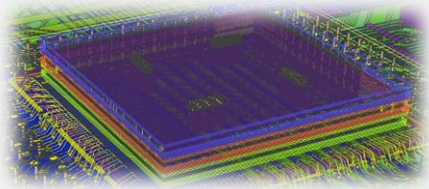
네패스는 **백엔드 파운드리(Advanced Back-end Foundry)** 전문 기업으로서 시스템 반도체 산업의 미래를 앞당깁니다.



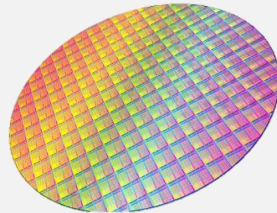


네패스는 FOPLP, nSiP 등의 첨단 반도체 기술로 글로벌 SCM의 지형을 바꾸고 있습니다.

### Semiconductor Supply Chain



IC Design



Silicon Fabrication



Package(WLP<sup>1</sup> / PLP<sup>2</sup>)



Final Test

IDM

OSATS

Fabless  
IC Players

Wafer Foundry

Bumping, RDL<sup>3</sup> Processing

Back-end Foundry



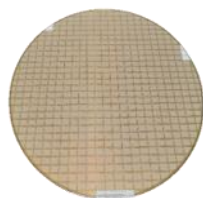
- <sup>1</sup> Wafer Level Package
- <sup>2</sup> Panel Level Package
- <sup>3</sup> Re-Distribution Layer

※ 2020년 국가핵심기술 지정



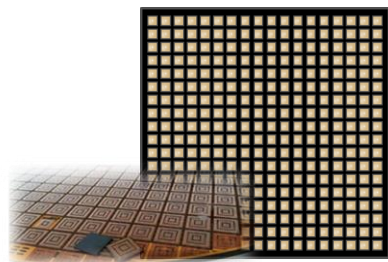
네패스의 End-fab 기술은 고성능 반도체를 경박단소화 하는 핵심 기술입니다.

Fan in WLP



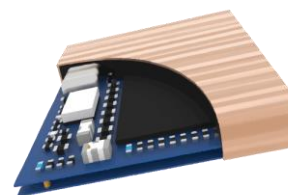
200mm / 300mm

Fan out WLP/PLP



300mm rd. / 600mm sq.

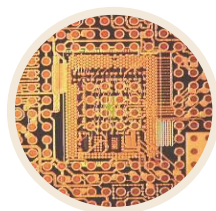
nSiP



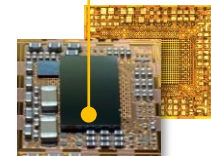
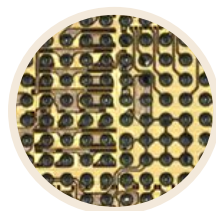
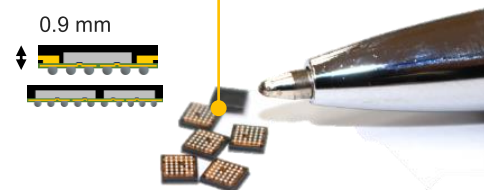
Small & Thin SiP(End fab+PLP)



0.4 mm



0.9 mm



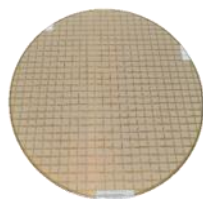
Applications



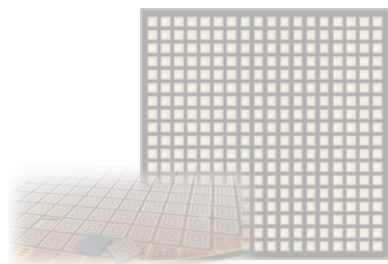


# CORE TECHNOLOGY | 01. Semiconductor ① WLP

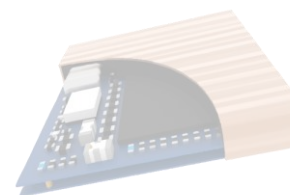
네패스의 End-fab 기술은 고성능 반도체를 경박단소화 하는 핵심 기술입니다.



200mm / 300mm

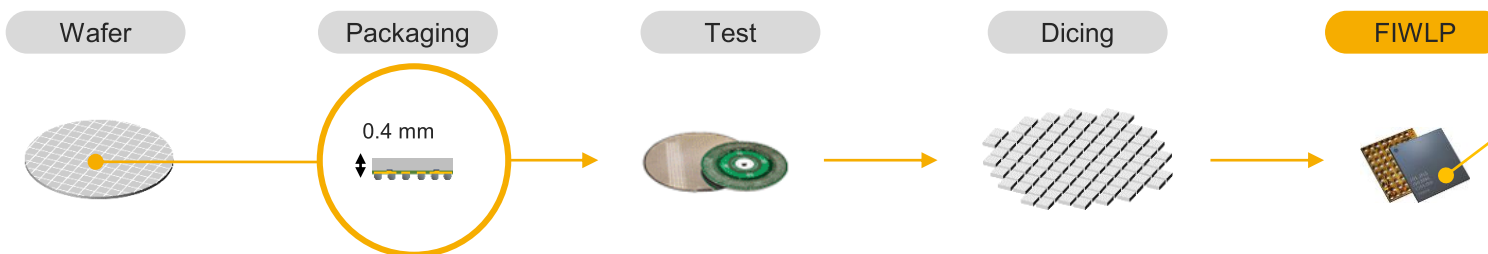


300mm rd. / 600mm sq.



Small & Thin SiP(End fab+PLP)

## ▶ FIWLP(Fan in Wafer Level PKG) Process



## Applications



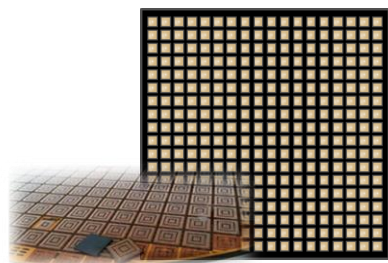


# CORE TECHNOLOGY | 01. Semiconductor ② FOWLP/PLP

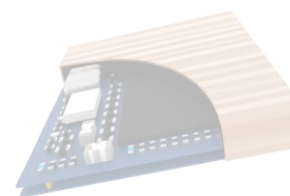
네패스의 End-fab 기술은 고성능 반도체를 경박단소화 하는 핵심 기술입니다.



200mm / 300mm

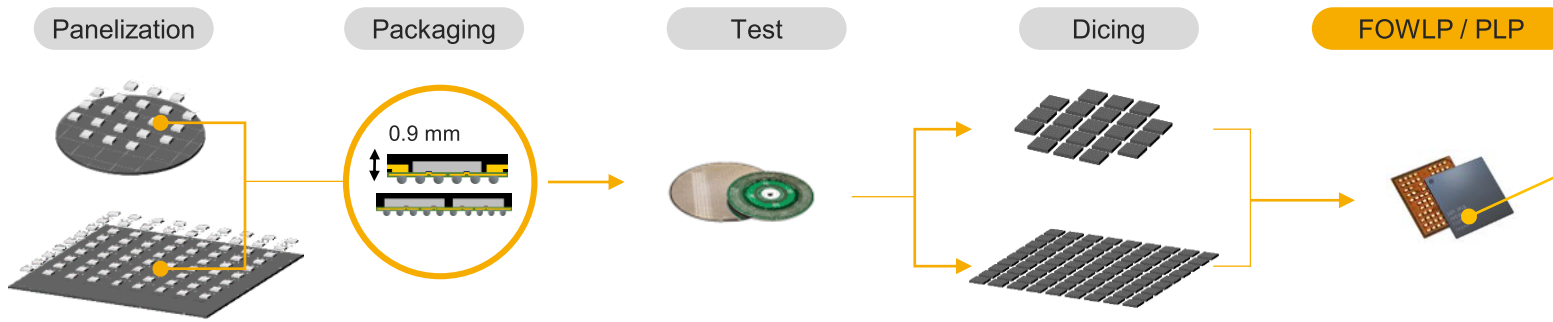


300mm rd. / 600mm sq.



Small & Thin SiP(End fab+PLP)

## ▶ FOPLP(Fan out Panel Level PKG) Process



## Applications





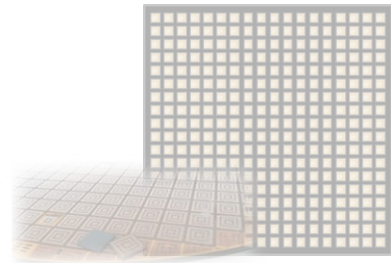


# CORE TECHNOLOGY | 01. Semiconductor ③ nSiP

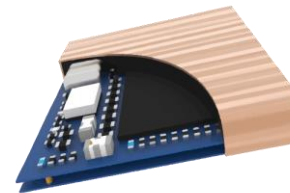
네패스의 End-fab 기술은 고성능 반도체를 경박단소화 하는 핵심 기술입니다.



200mm / 300mm

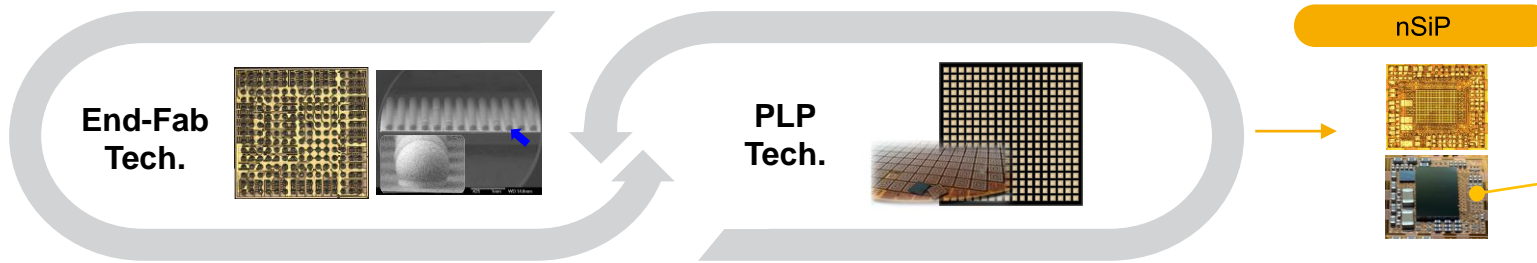


300mm rd. / 600mm sq.



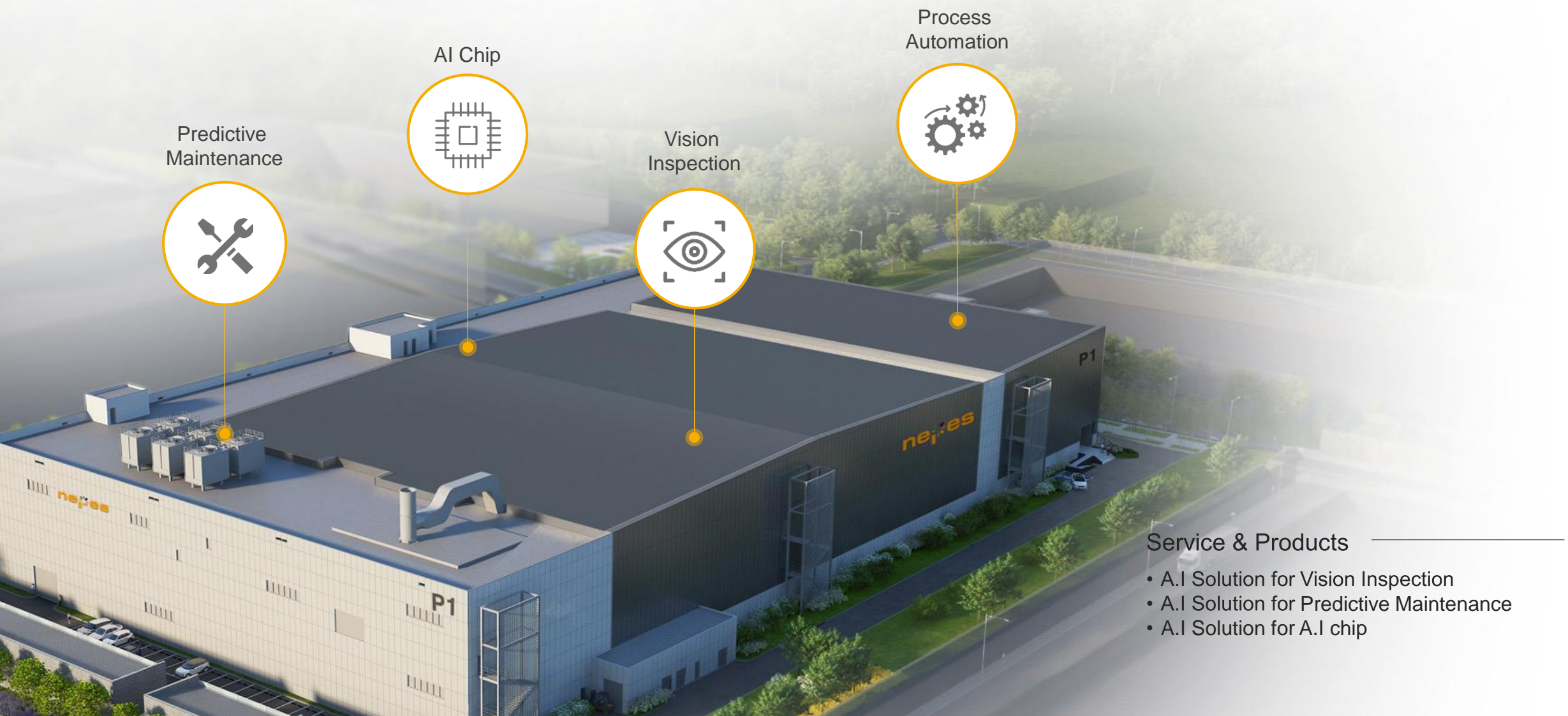
Small & Thin SiP(End fab+PLP)

## ▶ What is nSiP(System in PKG)?



## Applications

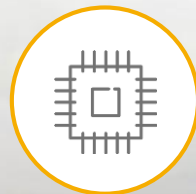




Predictive Maintenance



AI Chip



Vision Inspection



Process Automation



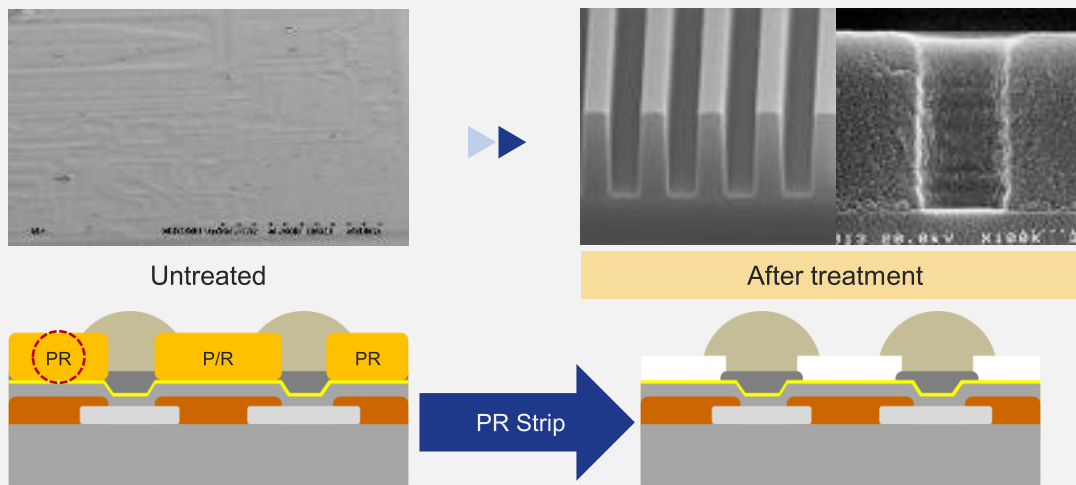
### Service & Products

- A.I Solution for Vision Inspection
- A.I Solution for Predictive Maintenance
- A.I Solution for A.I chip



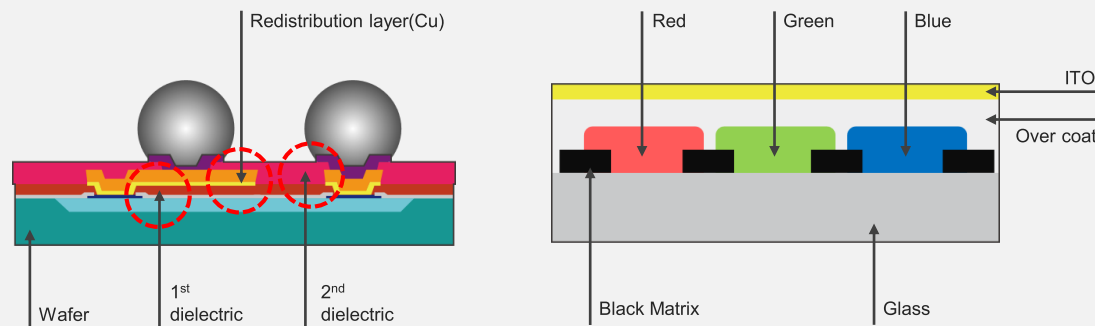
### Process chemicals

- PR
- Developer
- Stripper
- Etchant
- HSN



### Functional chemicals

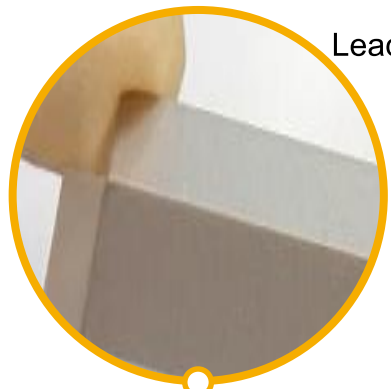
- ILD/PSPI
- Cu 도금액
- Color paste



### Applications



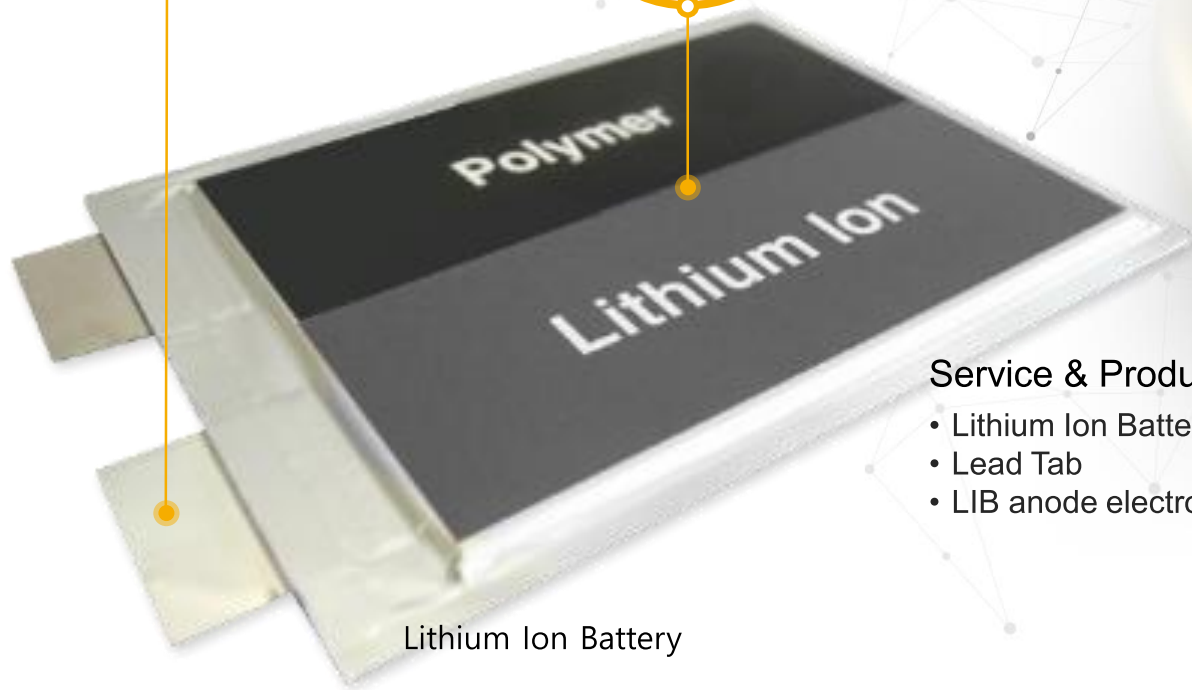
Semiconductor  
Display(LCD, OLED)  
Solar Cell



Lead Tab



LIB anode electrode

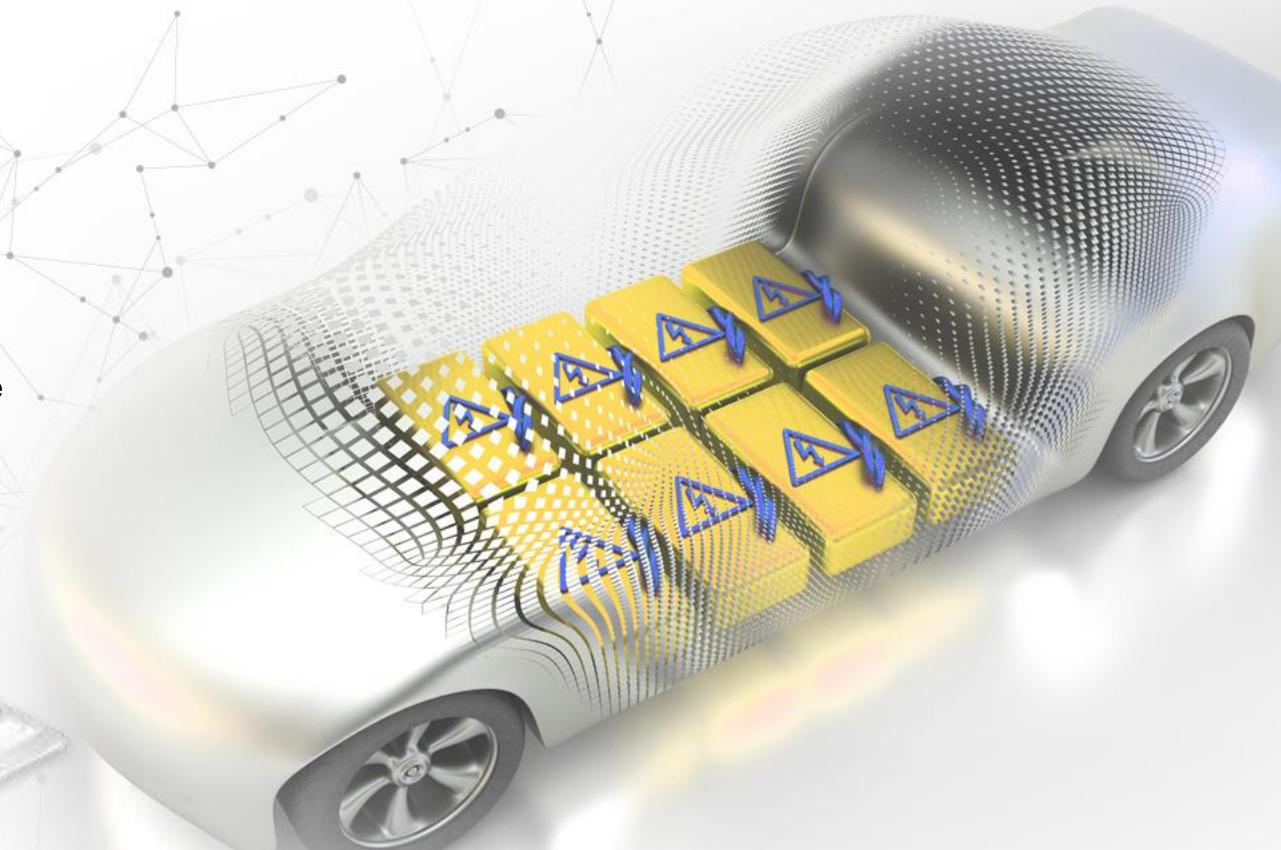


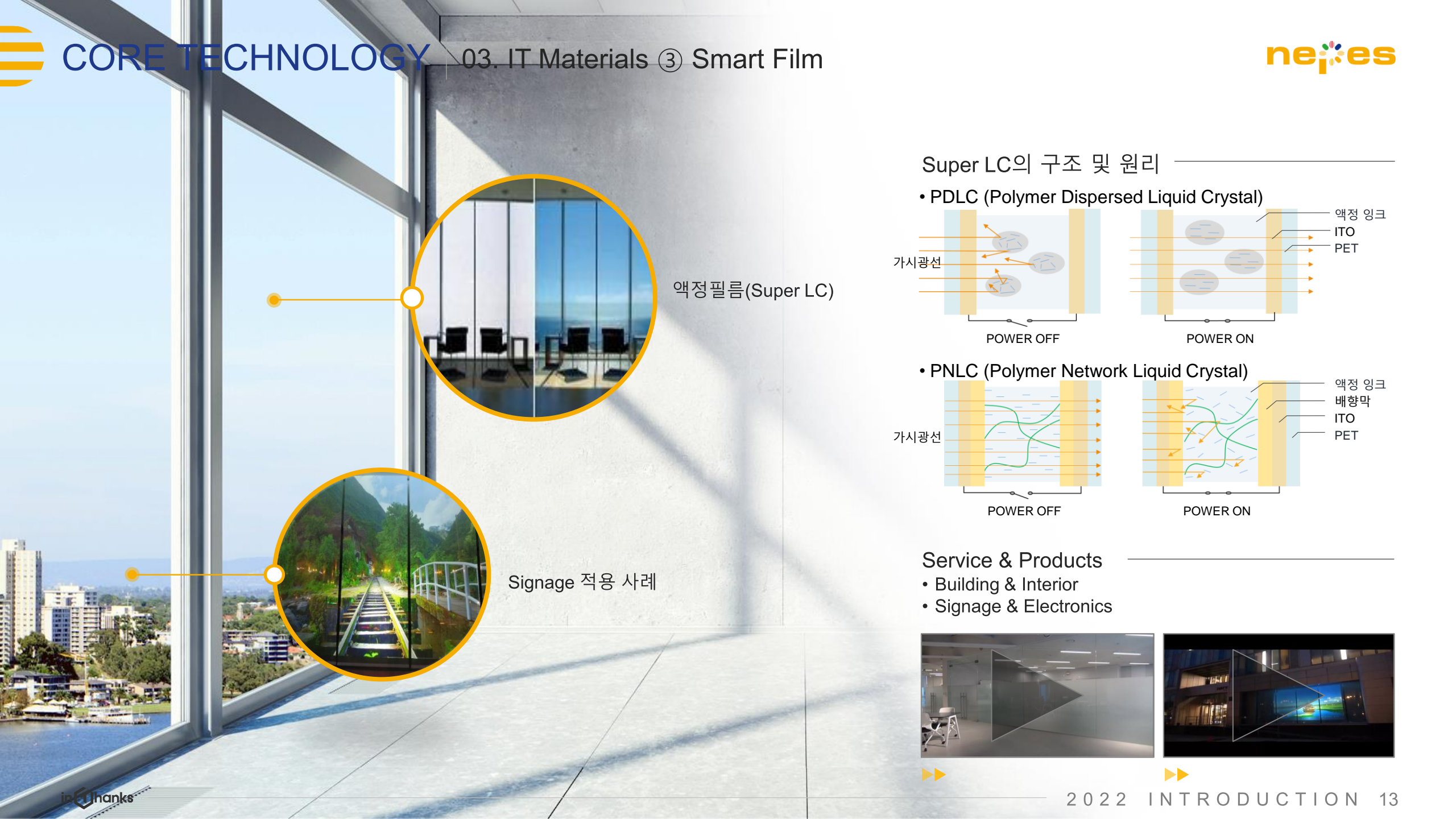
Lithium Ion Battery

### Service & Products

- Lithium Ion Battery
- Lead Tab
- LIB anode electrode

### Applications





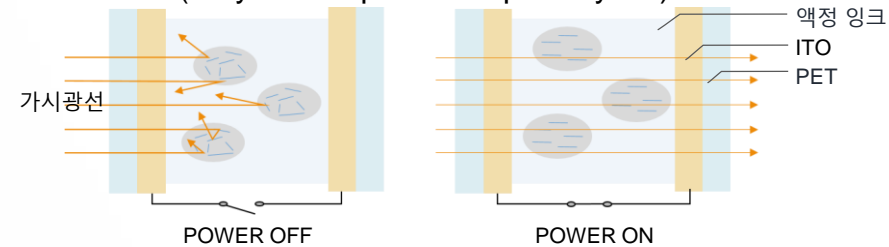
액정필름(Super LC)



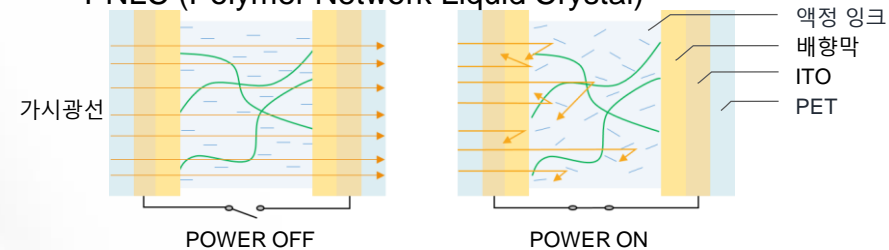
Signage 적용 사례

### Super LC의 구조 및 원리

#### • PDLC (Polymer Dispersed Liquid Crystal)

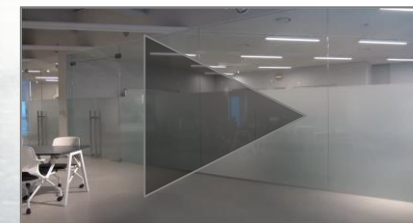


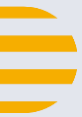
#### • PNLC (Polymer Network Liquid Crystal)



### Service & Products

- Building & Interior
- Signage & Electronics

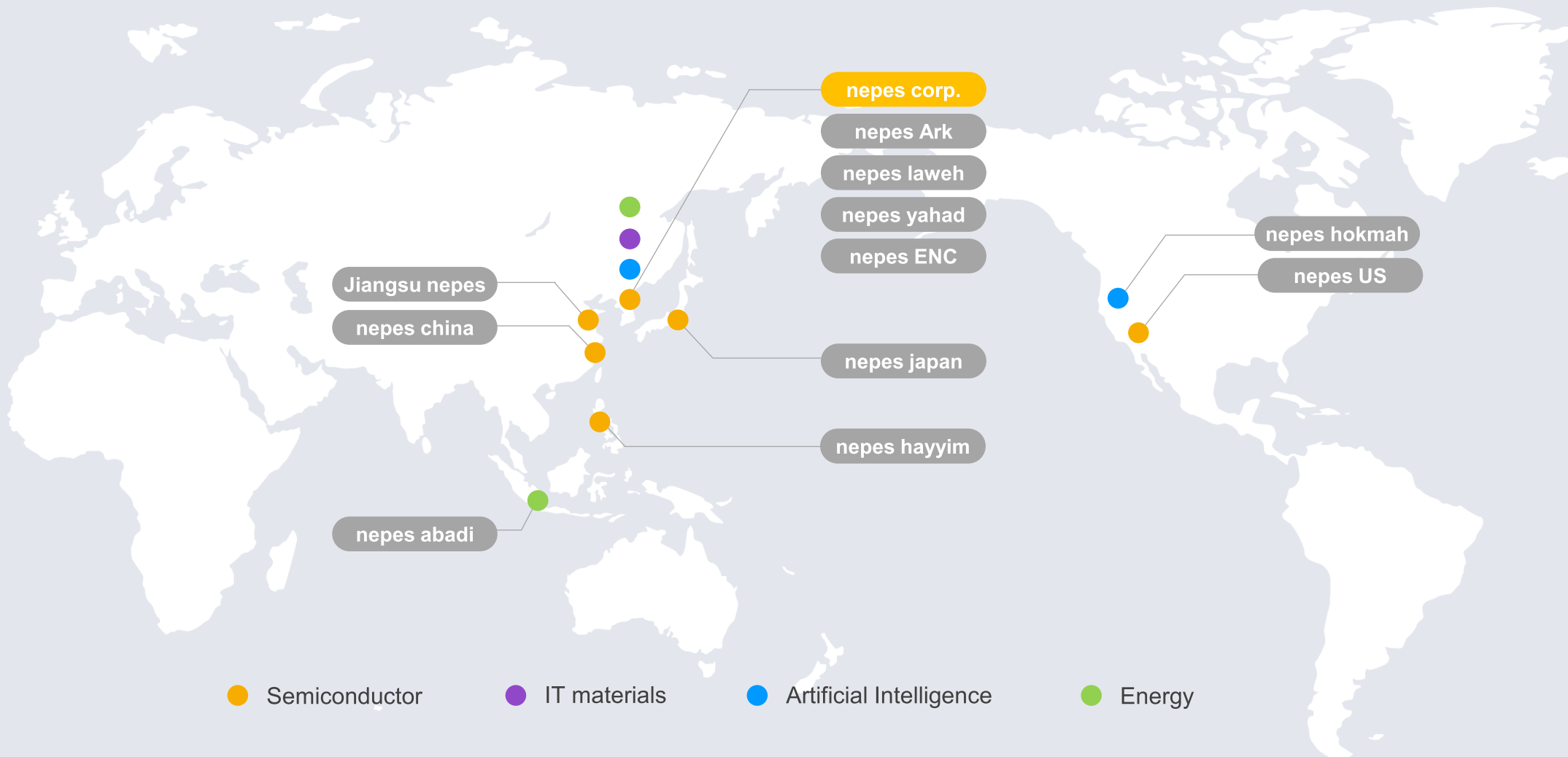




# GLOBAL NEPES



우리의 기술과 제품을 가지고 **땅끝까지** 섬기겠습니다.



- Semiconductor
- IT materials
- Artificial Intelligence
- Energy

네패스는 기업문화 증강으로 성과를 창출하여 **지속 성장**합니다.



# 3.3.7 LIFE

A close-up photograph of a dandelion seed head, with its seeds blowing away, set against a soft, golden sunset sky. The dandelion is the central focus, with its intricate structure of seeds and stems clearly visible. The background is a gradient of warm colors, from bright yellow near the horizon to a pale blue at the top.

**nepes**  
nepes corporation

THANK YOU

To Him who alone does great wonders, His love endures forever. Psalm 136:4

\* A dandelion means 'Gratitude' in the language of flowers

nepes corporation

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바이든 대통령의 행정명령으로 백악관이 21년 6월 반도체 공급망 조사 검토 보고서 발표

- 보고서에는 국가 안보에 중요한 첨단 패키징의 필요성을 강조하여 국내 반도체 제조 생태계 강화하자는 제안과 함께 글로벌 Top10 첨단 패키징 기업 중 하나로 네패스를 조명함



**BUILDING RESILIENT SUPPLY CHAINS, REVITALIZING AMERICAN MANUFACTURING, AND FOSTERING BROAD-BASED GROWTH**

100-Day Reviews under Executive Order 14017

June 2021

*A Report by*  
The White House

*Including Reviews by*  
Department of Commerce  
Department of Energy  
Department of Defense  
Department of Health and Human Services



**Advanced Packaging: Current Resilience** [43p.]

The top 10 advanced packaging companies include: two IDMs (Intel (U.S.) and Samsung (South Korea)); a foundry (TSMC (Taiwan)); the top five global OSATs (ASE Group (Taiwan), SPII (Taiwan), Amkor (U.S.), Powertech Technology (Taiwan), and JCET (China)) and two smaller OSATs: **Nepes (South Korea)** and Chipbond (Taiwan)). These 10 companies process approximately three-fourths of all advanced packaged chips.<sup>92</sup>

[Source: The White House, 'Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-based Growth', Jun '21]



# RECOGNITIONS 2 | Joining ASIC membership



IBM의 초청으로 22년 5월 American Semiconductor Innovation Coalition (ASIC)에 가입

- IBM 및 회원들은 네페스의 WLP 및 FOPLP와 같은 첨단 패키징에 대한 전문지식이 연합에 큰 가치를 제공할 것으로 기대



www.asicoalition.org

## Coalition Members Include





네패스만의 독특한 경영철학은 조직을 지속 성장하게 하는 창조적 경쟁력으로 인정받아 각종 국제 학술대회에서 우수 경영 사례로 소개

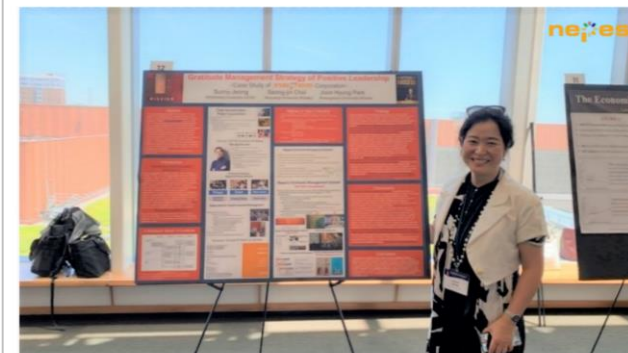
## 2022 GLOBAL CONFERENCE ON IHRM

**SAVE THE DATE! MAY 19-21, 2022**

## FIFTH GLOBAL CONFERENCE ON INTERNATIONAL HUMAN RESOURCE MANAGEMENT



**CIHRS**  
Center for International  
Human Resource Studies



Professor Sunny Jeong (Wittenberg University) presented the case of nepeas corporation.

Presented by:  
 MICHIGAN ROSS  
CENTER FOR POSITIVE ORGANIZATIONS

May 20, 2022 @St.John's Univ.  
Global Conference on  
International HR Management

June 22-23, 2022 @ Michigan Univ.  
Global Conference on Positive  
Organization



Market Trend

Smaller form factor  
(Based on Wafer-Level Platform)

Highly integrated Wafer-Level System in Package

Tech. Roadmap

Conventional PKG	Bumping	WLP	Fan-out WLP/PLP	System in PKG
<p>1.4mm</p> <p>Chip</p> <p>QFP</p> <p>QFN</p> <p>FCBGA</p>	<p>Gold</p> <p>Solder</p> <p>Etc(Cu Pillar, CNA bumping)</p>	<p>8"WLP</p> <p>12"WLP</p> <p>Chip 0.4mm</p>	<p>nPLP™</p> <p>600x600mm</p> <p>Chip 0.9mm</p>	<p>Multi-Chip Packaging</p> <p>System in packaging</p> <p>One Package Module</p> <ul style="list-style-type: none"> <li>- AP, PMIC</li> <li>- Flash Memory</li> <li>- Neuromorphic</li> </ul>

Position

Other OSAT

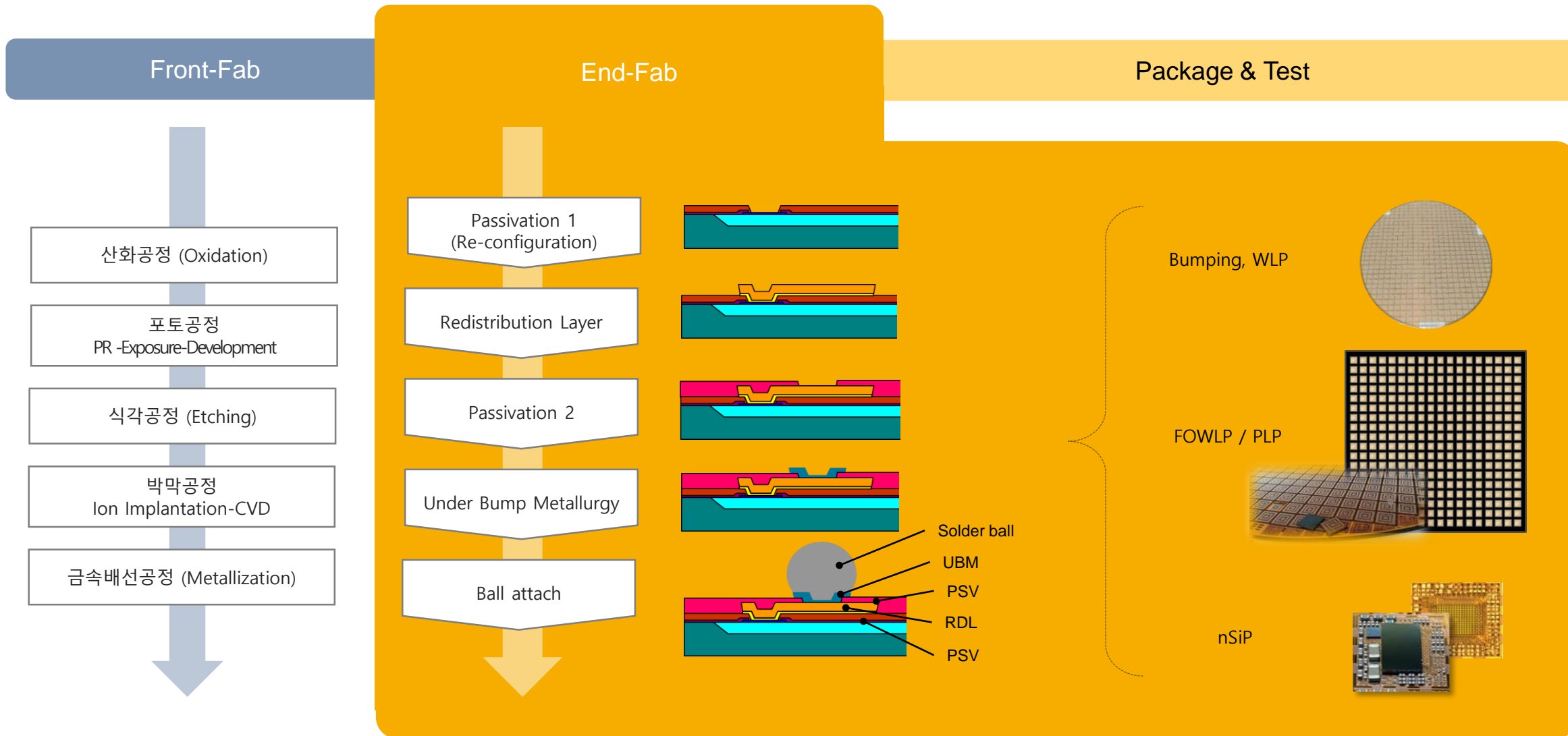
Conventional wire bonding packaging & Typical WLP technology

# nepes

## Back-end Foundry

(Bump, WLP, FOWLP, FOPLP, nSiP, TEST)

Front-Fab 공정 이후 Passivation, RDL 공정 및 Bump 공정을 지칭합니다.



# APPENDIX 3 | What is FOPLP?

- 네패스의 FOPLP는 업계 최대의 Panel 크기로 새로운 패널 표준입니다.
- FOWLP 경험과 재료 내재화, End-Fab 기술을 바탕으로 독자 FOPLP 기술을 확보하였습니다.

